



METHODICA
TECHNOLOGIES

New Eagle Raptor Summit

Towards Centralize Compute: Bridging Advanced Controls with AI

09/22/2025
v9.0



Company Overview



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Methodica Holdings and Subsidiaries



METHODICA HOLDINGS

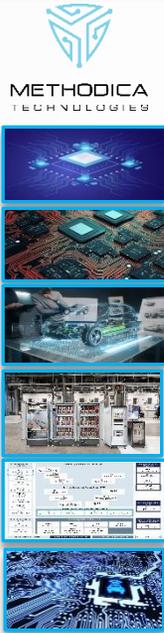
- HUMAN RESOURCES
- OPERATIONS
- IMMIGRATION
- FINANCE

Methodica Holdings is a leading Corporation overseeing two specialized entities one dedicated to **Product / Project Engineering services** and the other focused on **Product Accelerator Services**.

With the commitment to excellence and innovation, we provide comprehensive solutions tailored to meet the evolving technology landscape of our clients, driving success in today's dynamic marketplace

Product Engineering Services

Product Engineering Services



- Embedded Software Services
- Hardware Design Services
- System Engineering Services
- Verification, Validation Services
- Process & Quality Assurance
- Cybersecurity Engineering Services

TECHNOLOGY

RESOURCES



Western Labs brings all the products and services of Methodica Technologies but is structured to work in the defense and aerospace sectors.



About Us

Methodica Technologies is an **ISO-certified**, advanced mobility technology solutions and services company.

Our mission is to become the **go-to partner for customers focused on smart and efficient mobility**. We augment and complement our customers in key phases of the entire product development engineering cycle.

Engineers in
Product Development

250+



22+

Vehicle Program
Contributions

Global Clients
(NA, EUR, UK, CA)

15+



7

Continents with
Business In

Years of Exp. in
Mobility Development

15+



12+

Average Engineers
Experience



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Engineering Services Overview

Requirements

Requirements Elicitation

Architecture Design MBSE

HW Development

Prototype PCB Layout

Schematic Design

- ✓ Napkin Schematic - Prototype - Production Design
- ✓ Manufacturing for Low – Mid Volume
- ✓ Performance Simulation
- ✓ Design for Manufacturing & Optimisation
- ✓ Power Electronics Design, Simulation & Optimisation

SW Development

AUTOSAR Non-AUTOSAR

Model Based Development

- ✓ Comprehensive Software Development Lifecycle Framework (SWE.1 – SWE.4)
- ✓ Boot Loader Development to SW Unit Testing
- ✓ SDV platform Development
- ✓ SOC SW Development & Optimisation

Process and Quality Assurance

ISO26262 Functional Safety ISO21434 Cyber Security ISO42001 AI ML Systems



AUTOMOTIVE SPICE®

Assessment Implementation Validation

Verification & Validation

Test Methodologies

Unit Testing SIL HIL MIL VIL

E/E ADAS

- Plant Model Development
- HIL Design, Fabrication & Commissioning

Test Development

- Test Plan & Procedure Development
- ISTQB based System Engg. & Review
- Test Execution and System Analysis
- Test Automation

Our Products



All-in-one ADAS Camera, Radar and Lidar Data “Logging and Replay” HIL



Automotive Test Automation Platform Providing Cross Platform Test Scenarios

Domain Experience



Electric Drive Unit



Engine



ADAS



BMS



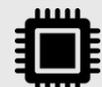
Brakes



Transmission



Infotainment



Software Defined Vehicle



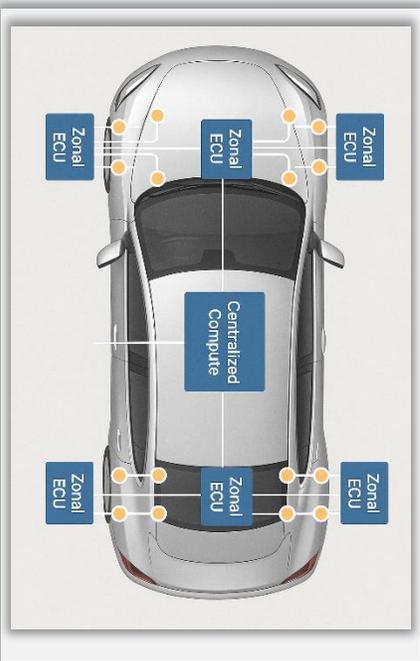
Overview

GPU-AMU Synergy

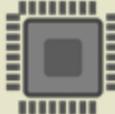


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Introduction & Motivation....



Market & System Drivers

- **Centralized compute & zonal E/E:**
Stricter latency and bandwidth budgets 
- **Explosion of sensors & AI**
Vision/LiDAR/radar need massive parallelism
- **Safety & determinism**
Braking/steering/powertrain need hard real-time
- **Model churn & OTA** 
AI evolves; control stack must remain stable
- **Thermal & power constraints**
Efficiency is non-negotiable
- **Business pressure**
Faster integration, lower BOM/wiring, scalable features

Architectural Response

- **Separation of Concerns**
AMU, MCU for Controls, GPU for Perception
- **Safety Island Supervision**
Watchdogs, Plausibility Checks, Degradation
- **Data Contract**
Time-Stamped, AMU, MCU never blocks GPU,
- **Data Communication , Synchronization**
Shared Memory, DMA, QoS, CRC-Checked
Shared memory
- **Future- Proofing** 
OTA on GPU, AMU, Micro remains
certified and deterministic

UC Control Loop $\leq 1\text{ms}$

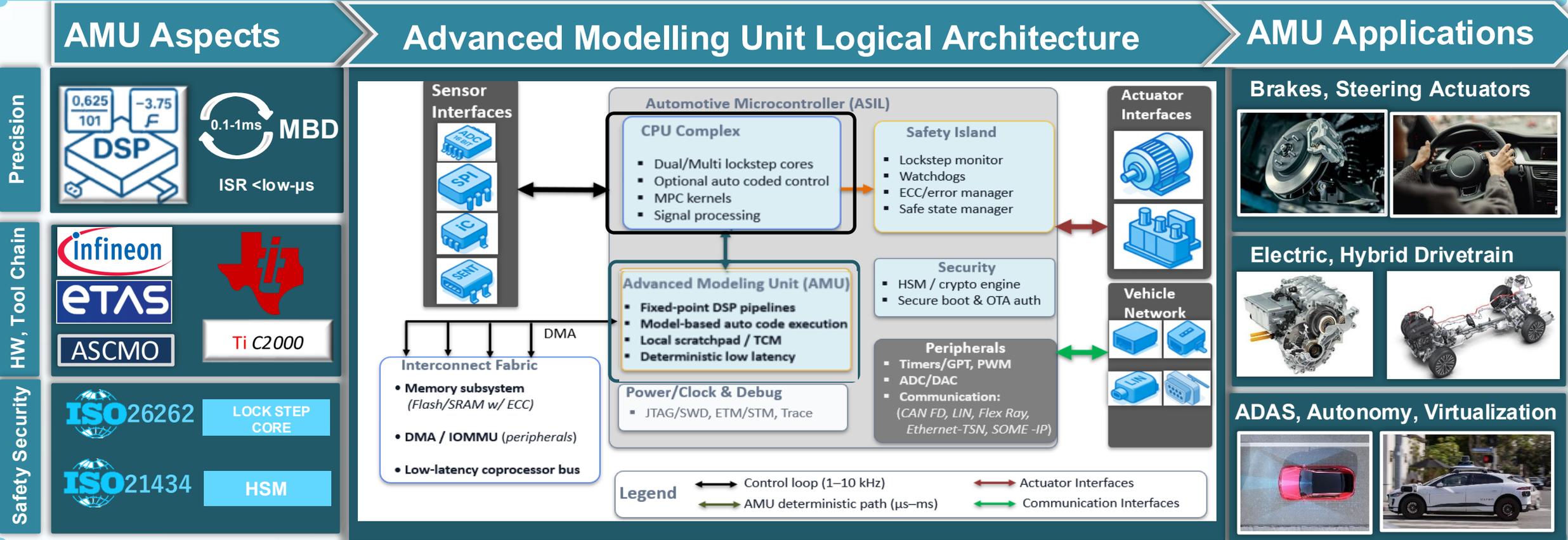
ADAS $\leq 1\text{ms}$

GPU \rightarrow AMU :20-30HZ

VEHICLE $< 300\text{ms}$



AMU(Advanced Modelling Unit) Overview..



Brakes, Steering Actuators



Electric, Hybrid Drivetrain

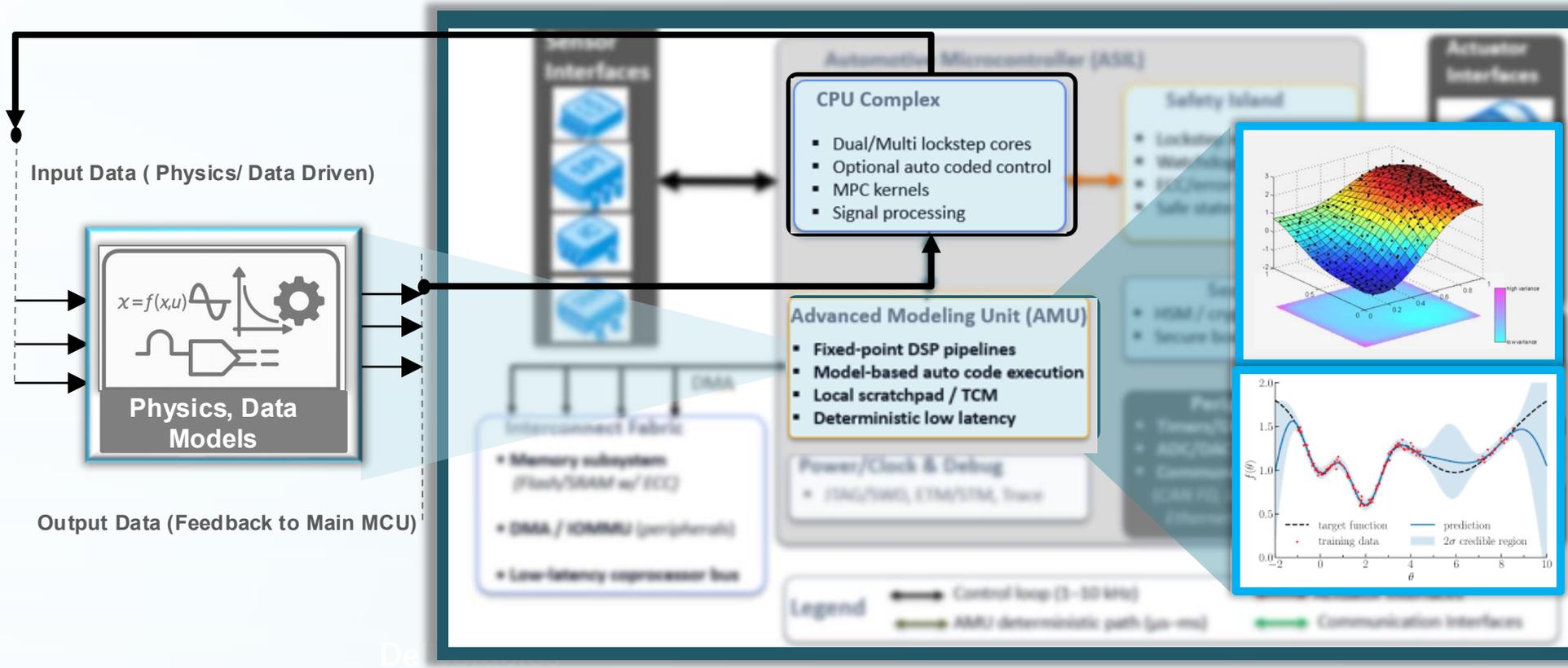


ADAS, Autonomy, Virtualization



- Specialized **hardware accelerator** within MCUs with Fixed or Floating-point capabilities.
- Already Available with Production MCU's such as infenion, TI, Nxp etc....
- ASIL-capable, lockstep cores, ECC, windowed watchdogs

AMU(Advanced Modelling Unit) Overview..

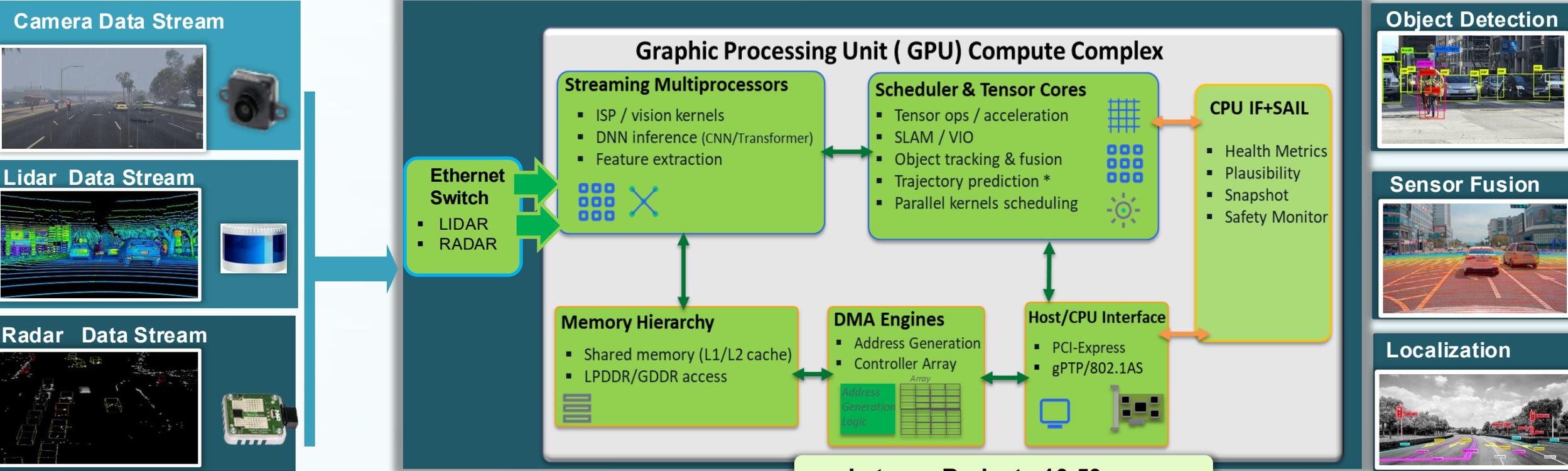


- Motor , Engine Torque, Speed, Thermal Estimations
- Sensor Virtualization estimation models
- Advanced MPC , GPR(Gaussian Process Regression)based models for Realtime Calibration coefficient, Values

- Can run high fidelity Advanced Controls, Data Driven Models
- Virtualization or In-Loop Plant , to provide Real time co-estimation of outputs such as Torque, speed
- Low latency, power efficiency, deterministic execution, real-time control, specific task optimization
- Typical loop times is a derivative of Resident Micro



GPU [Graphic Processing Unit] : Perception/AI Domain



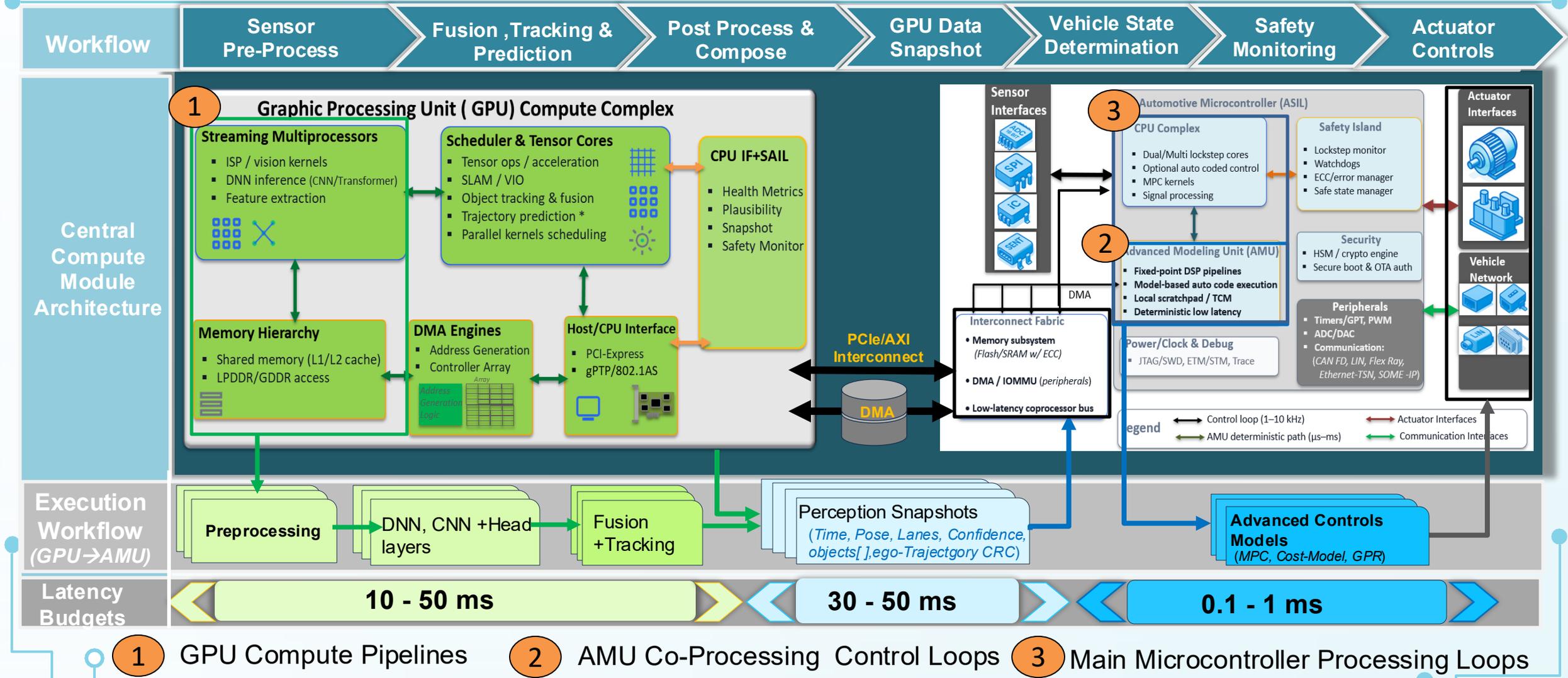
- Ability to Ingest Large Multimodal raw data streams
- Ability to Achieve **Massive Parallelism** in handling Multimodal data: CNN, Transformer, Fusion etc.
- Generate Perception heads such as Object detection, boundaries, depth, segmentation, localization & tracking
- Convert the interpreted data into Perception snapshot (ego –pose, lanes, objects, trajectory, CRC, time etc....)

AMU vs GPU: Comparison Table

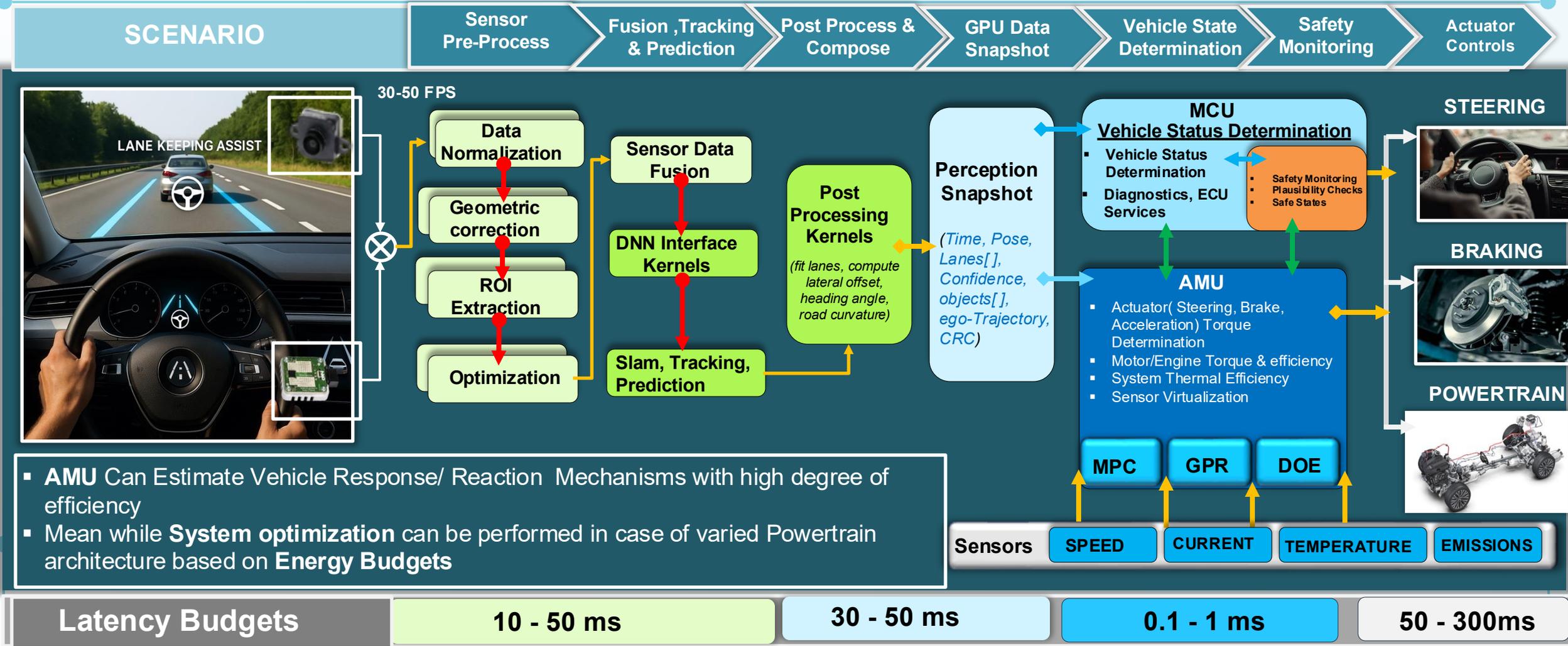
Key Attributes	Micro Controller(MCU), AMU	Graphic Processing Unit Complex (GPU)
Timing Model	Real Time, Control loops of 0.05 – 1ms, ISR latency in low- μ s , WCET via static scheduling.	Frame pipelines 10–50 ms typical, latency variance from scheduling, memory contention, thermal.
Safety & ASIL	Designed for ISO 26262 paths (lockstep, ECC, diagnostics, watchdogs); easier FFIs & safety cases.	Non ASIL-domain; supervised by safety island/MCU; safety via monitors, plausibility checks
Data Precision	Fixed-point, FP32/FP16 as available	FP32/FP16/BF16/INT8 (tensor cores/DP4A)
Latency Budgets	Inner loop: 0.5–1 ms ; command path: 3–10 ms .	Perception frame: 10–50 ms ; fusion/prediction: 5–20 ms per stage.
Fault Modes	ECC errors, watchdog resets, Safe States(deterministic)	OOM, TDR/timeouts, kernel launch failures, thermal throttle
Thermal & Power	Low–mid power; predictable thermal envelope	High dynamic power; thermal throttling can alter timing. requires power capping and perf governors.
Best Fit Functions		



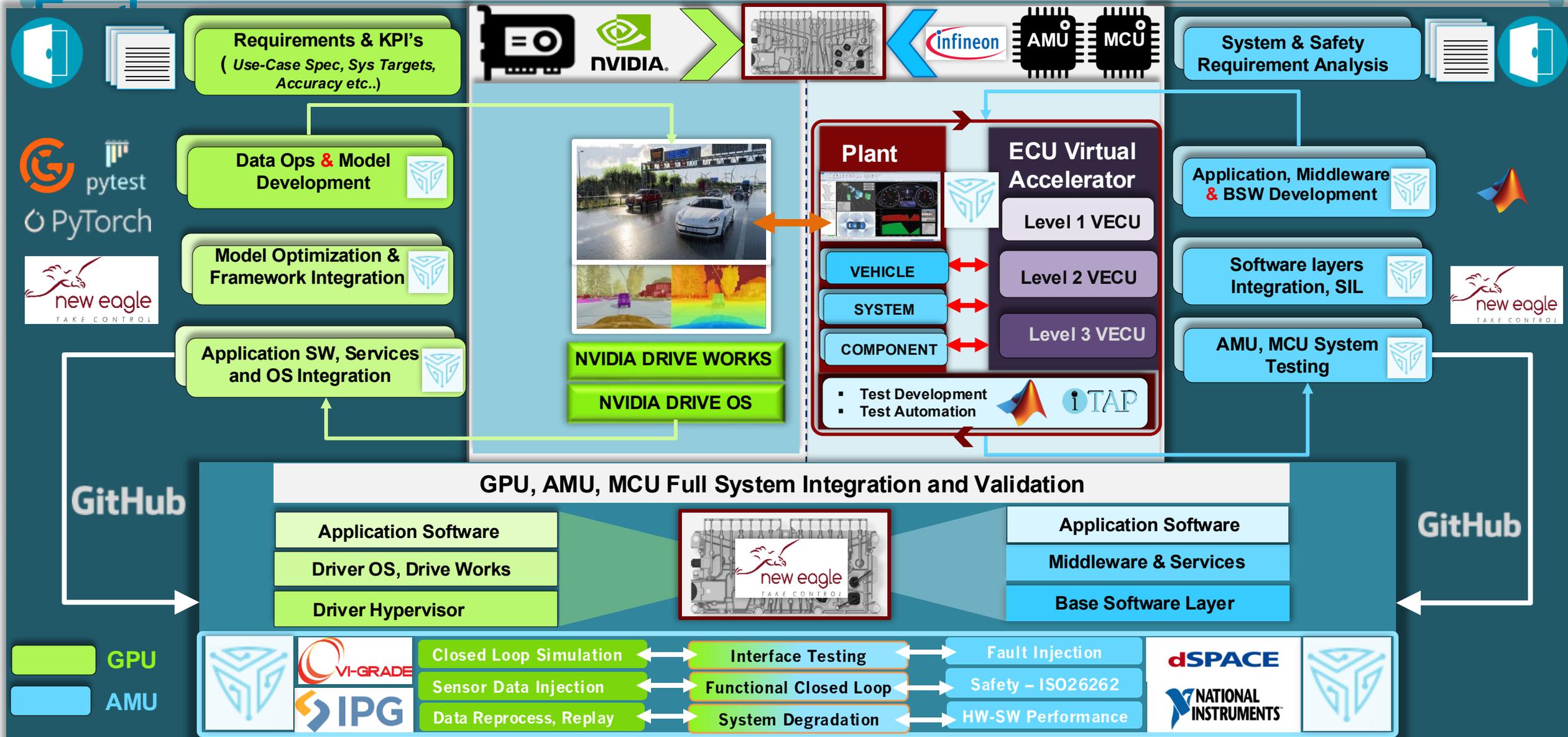
System Architecture : GPU, MCU, AMU



GPU-MCU-AMU Execution Pipeline Example: LDP/ACC



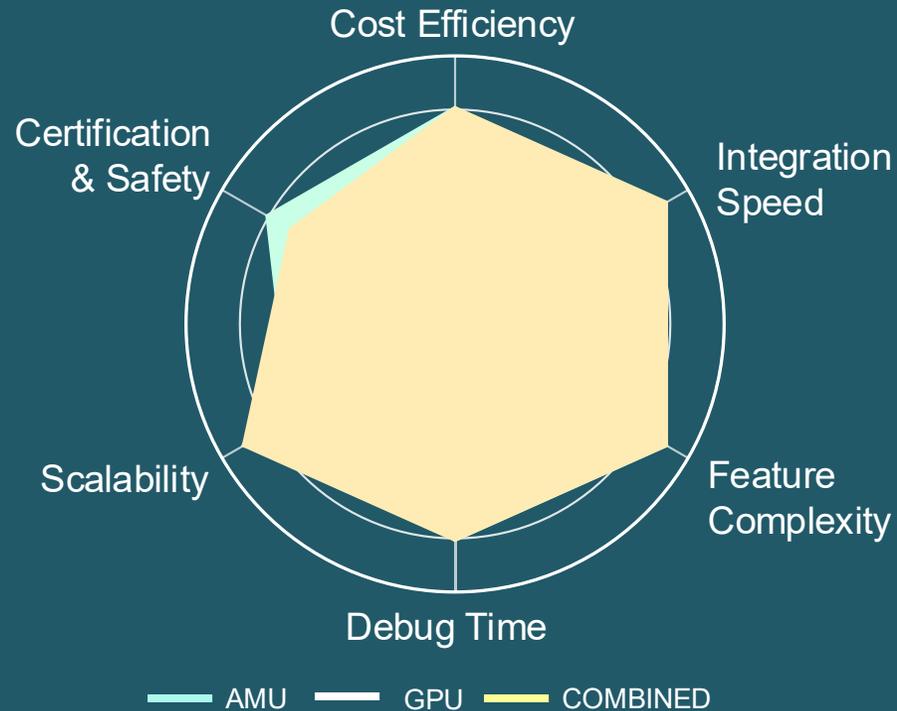
Development & Verification Flow: MTech <> New



Business Benefit Matrix: Best of Both the Worlds

1. **Low-mid silicon/power**; leverages ASIL-ready MCU platforms
2. Model-based control; **HIL/SIL** → **weeks not months**
3. **Deterministic loops** keep safety-critical scope contained
4. **Traceable timing**; reproducible **WCET** → faster root cause
5. Scales by **adding loops/functions** on same MCU family

1. **Higher silicon/power**; replaces multiple perception ECUs
2. **Modular models & toolchains**; OTA model drop-ins
3. **Throughput tasks isolated**; can innovate without recertifying control
4. **Nsight/profilers + golden sets**; faster perf bottleneck
5. Scales with newer **GPUs**, quantization, partitioning (MIG/MPS)



1. Net BOM ↓ via ECU consolidation + predictable thermal budget
2. Parallel tracks (**control vs AI**) cut integration lead-time by **30–50%**
3. Clear interface (“**Perception Snapshot**”) reduces **cross-team** coupling
4. Fault isolation: **GPU issues** don’t block **AMU validation**
5. Independent scaling: **upgrade GPU without redoing** AMU safety case

Integration Lead Time
↓ 30–50%

BOM, Power Budget
↓ 10–25%

Debug, Validation
↓ 25–40%



Roadmap & Outlook...

Current : Foundation for hybrid AMU-GPU stack

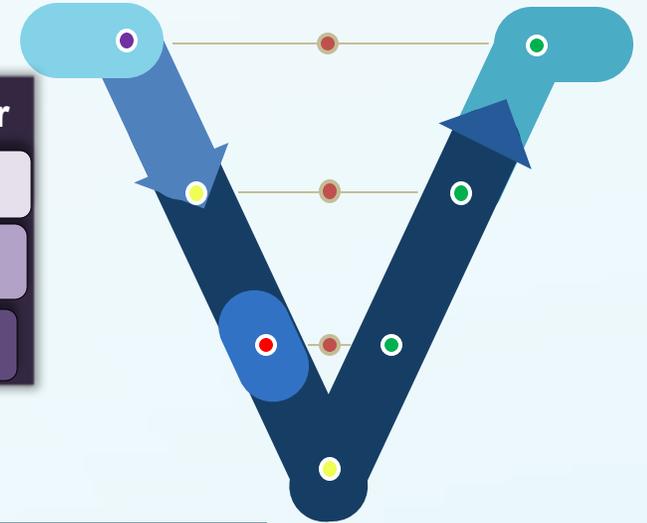
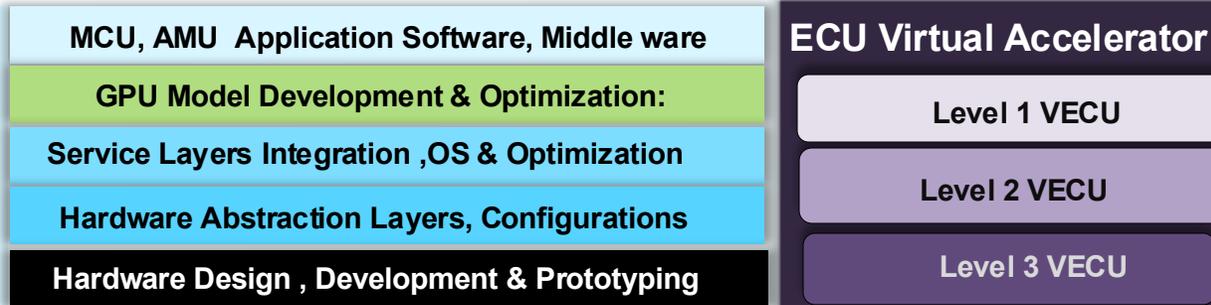
Yr-2028 : Cost and integration gains begin compounding, Reuse & TTM

Yr -2030+ : Architecture evolution in safety certification readiness



Methodica as a Technology Partner(Dev & Integration)

Product Development Work Packages



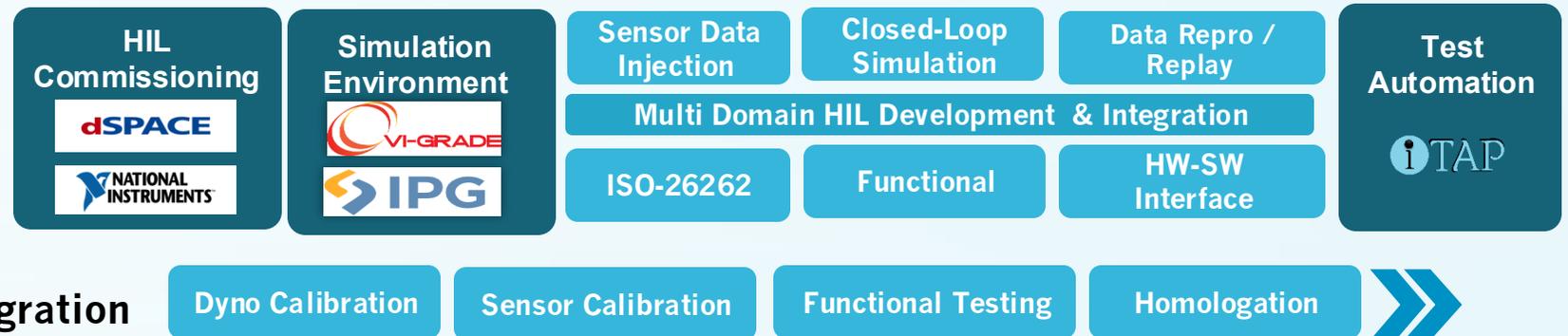
- ❑ Complete Support of Application Stacks, Software development for **MCU,AMU & GPU**
- ❑ **vECU, vGPU** Platform setup, Simulation, Integration and Verification

Product Integration & Validation Activities

➤ **Hardware-in-the-Loop ADAS**

➤ **Hardware-in-the-Loop MCU, AMU**

➤ **System Calibration & Vehicle Integration**





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